WHAT IS CLAIMED IS:

1. A method of manufacturing a thin film transistor array panel for a liquid crystal display, the method comprising:

forming a gate wire including a gate line and a gate electrode connected to the gate line;

depositing a gate insulating layer;

forming a semiconductor layer;

forming a data wire including a data line intersecting the gate lines to define a pixel area, a source electrode connected to the data line and placed close to the gate electrode, and a drain electrode placed opposite the source electrode with respect to the gate electrodes;

depositing a protective layer covering the gate wire or the data wire;

forming an organic insulating layer by spin-coating an organic insulating material on the protective layer;

patterning the organic insulating layer to form a first contact hole exposing the protective layer opposite the drain electrode;

surface-treating the organic insulating layer by plasma process using inactive gas;

patterning the protective layer to form a second contact hole exposing the drain electrode and located inside the first contact hole; and

forming a pixel electrode electrically connected to the drain electrode through the first and the second contact holes.

2. The method of claim 1, wherein the pixel electrode comprises a transparent conductive electrode or a reflective conductive film.

3. The method of claim 2, wherein a surface of the organic insulating layer has an unevenness pattern when the pixel electrode has the reflective film.

4. The method of claim 2, wherein the reflective film has an aperture in the pixel area when the pixel electrode comprises both the transparent electrode and the reflective film.

5. The method of claim 1, wherein the semiconductor layer comprises amorphous silicon or polysilicon.

6. The method of claim 1, wherein the gate wire further includes a gate pad connected to one end of the gate line, the data wire further includes a data pad connected to one end of the data line, and the protective layer or the gate insulating layer has a third contact hole exposing the gate pad or the data pad, and wherein the thin film transistor array panel further comprises a subsidiary pad electrically connected to the gate pad or the data pad through the third contact hole and including substantially the same layer as the pixel electrode.

7. The method of claim 1, wherein both the data wire and the semiconductor layer are formed by a photo etch step using a photoresist pattern with position-dependent thickness.